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P2.16 A PROGRAMMABLE REAL-TIME DATA PROCESSING AND DISPLAY SYSTEM FOR THE NOAA/ETL DOPPLER RADARS

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1. INTRODUCTION

NOAA's Environmental Technology Laboratory (ETL) has been developing and testing a dual-use atmosphere and ocean sensing radar for three years. Because this dual-polarized, variable pulse width, X-band radar can scan negative, as well as positive, elevation angles, it has been used in two field projects for observing ocean surface features (Kropfli and Clifford, 1996), and numerous projects for over 15 years where it performed only as an atmospheric radar.

The expanded capabilities of this radar require a new data acquisition system that allows the radar to take data faster than previous systems and to calculate several additional parameters. With these new parameters come increased demands for real-time recording and display options. In the past the NOAA/ETL atmospheric Doppler radars have had more limited real-time acquisition and display capabilities (Moninger, 1983; Gibson and Martner, 1995).

2. The Radar Acquisition and Display System

The Radar Acquisition and Display System (RADS) is a transportable system designed to record and display data from a research Doppler radar with polarization diversity. Physically, the unit consists of a 6U VMEbus chassis, an external color monitor, keyboard and mouse.

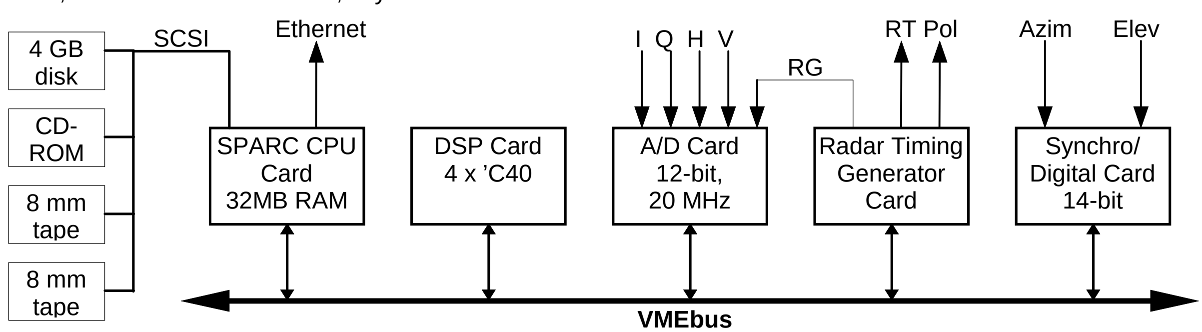

Figure 1. Radar Acquisition and Display System

Connection to the radar is made at four levels: radar timing signals (radar trigger and polarization control), receiver (in-phase and quadrature video, log output from both horizontally and vertically polarized receivers), synchro lines for monitoring azimuth and elevation, and Ethernet for directing antenna scanning (see Figure 1).

2.1 Hardware Design

All components of the system are purchased off-the-shelf except for one VMEbus card: the Radar Timing Generator (RTG). The RTG generates radar triggers, range gates and polarization control signals. Other VMEbus cards are a SPARC-based CPU, a DSP (Digital Signal Processing) card containing four TMS320C40 processors, a four-channel 20 MHz A/D card with buffer memory, and a synchro/digital card. The chassis also contains a hard disk drive, a CD-ROM drive, and two 8 mm cartridge tape drives.

2.2 Software Design

Software is divided into two parts: that which runs on the SPARC, and that which runs on the DSP card. The SPARC runs Solaris 2.5, which is an SVID-compliant (System V Interface Definition) UNIX. UNIX is not often thought of as a real-time operating system because of its long interrupt response time (among other reasons), however it has proven to be adequate for our purposes because of the capabilities of the DSP card to moderate and buffer the data flow. No operating system is used on the DSP card, which is programmed in C and assembly.

3. DSP Processing

In operation, a beam (or ray) of data is buffered in the A/D card, and is then transferred to the DSP card over VMEbus. The four identical processors on the DSP card each take a fourth of those data, divided by range gate, and perform a processing algorithm. If an auto-covariance algorithm (*e.g.,* pulse-pair) is performed, there is typically a factor of 15 or more reduction in the amount of data. Other algorithms, such as power spectrum, typically give only a factor-of-two reduction in the amount of data.

Data from this processing are buffered in the memory of the DSP for up to five beams. This amount of buffering has been found to work quite well, as long as the SPARC is not performing compute-bound activities, such as compiling, while it is also trying to acquire, display and record data. Each beam of data is tagged with a header that contains the time, azimuth,

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elevation and a serial number. These data are then transferred to the SPARC.

The DSP calculates data products for recording and for display. The display data products will be discarded by the SPARC after being displayed, since they can be recalculated from the recorded data products, and recording them to tape would restrict the data rates possible.

4. SPARC Processing

When the SPARC receives the data from the DSP, it first divides the data into record and display packets and affixes a Universal Format (UF) header (Barnes, 1980) to each. These packets are then sent to different processes.

The record process writes the data to 8 mm tape. The tape format is very similar to the UF tape format, except that the data are floating-point. A post-processing program converts these data to 16-bit integer to produce a true UF-format tape that can be read by existing software.

The display process separates data into FIFO (First In, First Out) buffers for each field that are maintained for 600 beams of data. The operator may select one field for display and that field is output to the screen. This process runs in a continuous loop, such that if beams of data come in faster than they can be displayed, all beams available will be drawn to the screen simultaneously. The operator can change fields and immediately see up to 600 beams. In PPI mode, this is normally enough data to display an entire rotation.

The RADS display subsystem has been modeled after the Auxiliary Radar Control System (ARCS) described by Gibson and Martner (1995). It has the capability of real-time areal displays of at least eight derived fields for PPI, sectors, RHI, and fixed-beam scans as they occur. It can also display real-time two- and three-dimensional plots of Doppler spectra, derived VAD fields (wind speed, directions, *etc*.) and delta-k and differential phase derived fields. No special hardware is required to generate the images.

The operator controls the radar through a GUI (Graphical User Interface) window on the color monitor. All radar parameters may be viewed, and certain subsets of parameters may be selected to be shown simultaneously on the screen. Thus if the RADS is in Pulse-Pair mode, only those parameters that are pertinent to that mode, and that are changed frequently in that mode, will be displayed. In addition, because of the large number of radar parameters (> 80), they are grouped by primary function (timing, calibration, scanning, transmit, receiver, data processing and housekeeping), and may be displayed by these groupings.

The operator may select functions through soft buttons on the GUI, and in this way controls scanning, processing and recording. The actual scan control is done by another VME-based computer that is resident in the radar. This computer communicates with RADS through Ethernet, however antenna position is read directly by RADS from the synchro signals.

5. Initial Uses and Advantages of RADS

RADS accompanied the Doppler radar system to the Coastal Ocean Probing Experiment in Oregon in August /September, 1995. At that time, the new system demonstrated the ability to take real-time delta-k data and display them. The system also recorded time series data. In Snowrad '96, the system provided real-time power spectrum displays of Doppler velocity in three different formats, and recorded pulse-pair data.

In the laboratory, the system has demonstrated the capability to process 512 range gates in a pulse-pair processing mode with 1.0 ms between 64 pairs. To date, the following modes have been programmed: time-series, spectrum, pulse-pair, delta-k, and a differential phase mode which includes horizontal-vertical correlation, $\rho_{HV}(0)$.

RADS provides several advantages over the previous system, particularly in terms of data rates and operating mode flexibility. The delta-k, Doppler spectra and differential phase capabilities, for example, are entirely new features. RADS is made almost entirely from off-the-shelf purchased components, which reduces development, replication and replacement costs. Since it is completely programmable, new algorithms can be readily implemented. Range gates can be spaced as closely as 7.5 m. Use of a modern computer and operating system allows a much more capable radar control program to be implemented.

One advantage of using the VMEbus is that it is a true multi-processing bus, which allows capabilities to be increased by adding more processing elements. The main limitation is a bus bandwidth of 80 MB/s. The only high bandwidth path in RADS is between the A/D and the DSP which, with the parameters previously given, is 8.2 MB/s. Thus, available bandwidth could support a second DSP and/or A/D card. Other possible cards make almost no demand on bandwidth because of the reduction in data volume provided by the DSP card.

6. Acknowledgments

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7. References

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